



Advanced Electronic Packaging: Volume 968 (MRS Proceedings)

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Microelectronic packaging architecture evolutions are being driven by silicon technology advancements and new form factors, used models and emerging technologies. High-performance mobile computer and communication systems will require higher I/O counts, greater density, lower cost, lighter weight and improved performance in the electronic package. The book focuses on silicon technology dimension scaling and performance improvement, Pb-free or 'green' assembly, and system-in-package (SIP) technologies. It explores the key thermomechanical failure modes and mitigating solutions associated with integration of silicon with weak interlayer dielectrics during the assembly process, under bump metallurgy integrity with lead-free assembly, and the impact of stress on die-cracking and transistor performance in 3D thin-die stacking. The interaction of these failures with silicon and assembly materials, processes and design features is covered and includes: system in package; advanced packaging/nanotechnology in packaging; physical behavior and mechanical behavior in packaging; electromigration and thermal behavior in packaging and thin films and adhesives in packaging.

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